CLAIMS

1. A method comprising:
detecting a condition of an integrated circuit having a TAP while communicating with the TAP using a first TAP control device; and
communicating with the TAP using a second TAP control device in response to detecting the condition.

2. The method of claim 1, wherein communicating with the TAP using a second TAP control device occurs in response to detecting the condition and issuing a second control signal to the second TAP control device.

3. The method of claim 1, wherein the condition is a failure of the integrated circuit.

4. The method of claim 1:
wherein the condition is associated with a set of state data in the integrated circuit; and
wherein communicating with the TAP using a second TAP control device, comprises reading the set of state data using the second TAP control device.

5. The method of claim 1, further comprising:
maintaining the integrated circuit in the detected condition; and
coupling the second TAP control device to the TAP while maintaining the integrated circuit in the detected condition.

6. The method of claim 5, wherein coupling the second TAP control device to the TAP occurs in response to a first control signal from the first TAP control device.

7. A method comprising:

inputting test data from a first memory device to a test-access port of an integrated circuit; and

storing state data associated with the input test data and output from the test-access port in a second memory device have a lower nominal speed rating than the first memory device.

8. The method of claim 7, wherein the first memory device stores vector test-pattern data and second memory device does not store.

9. The method of claim 7, wherein storing state data associated with the input test data occurs after:

detecting existence of a desired condition of the integrated circuit; and

decoupling the first memory device from at least a portion of the test access port.

10. A system comprising:

first means for communicating with a test-access port of an integrated circuit;

second means for communicating with a test-access port of an integrated circuit; and

a multiplexer module, coupled between the test-access port and the first means and between the test-access port and the second means, for selectively coupling the first or second means to the test-access port.

11. The system of claim 10:

wherein the first and second means include respective first and second sets of signal nodes for outputting or receiving signals from a test-access port; and

wherein the multiplexer module includes first and second multiplexers, with each multiplexer having a first input node coupled to one of the signal nodes in the first set of signal nodes and a second input node coupled to one of the signal nodes in the second set of signal nodes.

12. The system of claim 10, further comprising means for communicating a control signal from the first means to the second means to coordinate control of the test-access port.

13. The system of claim 10, wherein the first and second sets of signal nodes output or receive respective sets of JTAG signals.

14. Apparatus comprising:

a first TAP control device having a first node for connection to a test port of an integrated circuit; and

a multiplexer including first and second selectable nodes and a non-selectable node, with the first selectable node coupled to the first node of the first TAP control device and the non-selectable node for connection to the test port.

15. The apparatus of claim 14, further comprising a second TAP control device having a second node coupled to the second selectable node of the multiplexer.

16. The apparatus of claim 14, further comprising a vector pattern memory or algorithmic pattern generator coupled to the first TAP control device.

17. The apparatus of claim 14, wherein the first TAP control device comprises a JTAG boundary-scan controller.

18. Apparatus for selecting control of a test-access port of an integrated circuit, comprising:

first means for electrical connection to a node of a first TAP control device;

second means for electrical connection to a node of a second TAP control device;

third means for electrical connection to a node of a test-access-port of an integrated circuit; and

a first multiplexer coupled to the first, second, and third conductive means for selectively coupling the first or second means to the third means for electrical connection.

19. The apparatus of claim 18, further comprising a circuit board supporting the first multiplexer and the first, second, and third means.

20. The apparatus of claim 18, wherein the third means is for connection to one of a test clock node, a test-data-input node, a test-mode-select node, and a test-data-out node of the test-access port.

21. The apparatus of claim 18, further comprising:

fourth means for connection to a node of the first TAP control device;

fifth means for connection to a node of the second TAP control device;

sixth means for connection to a node of the test-access-port; and

a second multiplexer coupled to the fourth, fifth, and sixth conductive means for selectively coupling the fourth or fifth conductive means to the sixth conductive means.

22. Apparatus comprising:

a first connector for connection to a first TAP control device;

a second connector for connection to a second TAP control device;

a third connector for connection to a test-access-port of an integrated circuit; and

a first multiplexer coupled to respective first, second, and third nodes of the first, second, and third connectors for selectively coupling the first or second nodes to the third nodes.

23. The apparatus of claim 22, further comprising a circuit board supporting the first multiplexer and the first, second, and third connectors.

24. The apparatus of claim 22, wherein each of the first, second, and third connectors includes a test clock node, a test-data-input node, a test-mode-select node, and a test-data-out node.

25. A machine-readable medium including coded instructions for operating a switching device to couple one of a plurality of TAP controllers to a TAP in an integrated circuit.

26. The machine-readable medium of claim 25, further including coded instructions for operating a device to detect a condition of the integrated circuit while using a first TAP controller and for communicating with the TAP using a second TAP control device in response to detection of the condition.

27. The medium of claim 25, wherein the condition is a failure of the integrated circuit.

28. The medium of claim 25, wherein the medium comprises an electronic, optical, or magnetic memory.